We claim:

1. A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source, a first pair of potentials having a relatively small potential difference; and

a second logic gate using, as an operation power source, a second pair of potentials having a relatively large potential difference,

wherein substrate potentials of MIS transistors are commonly used by said first and second logic gates.

2. A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

3. A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a forward

direction by said substrate potential.

4. A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

5. A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential.

6. A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source, a first pair of potentials having a relatively small potential difference; and

a second logic gate using, as an operation power source, a second pair of potentials having a relatively large potential difference,

wherein each of said first and second logic gates has an MIS transistor, and a well region of the MIS transistor in which

said first logic is formed and a well region of the MIS transistor in which said second logic gate is formed are made common every conduction type.

7. A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source, a first pair of potentials having a relatively small potential difference; and

a second logic gate using, as an operation power source, a second pair of potentials having a relatively large potential difference,

wherein each of said first and second logic gates has an MIS transistor, and a well region of the MIS transistor in which said first logic gate is formed and a well region of the MIS transistor in which said second logic gate is formed are electrically made conductive every conduction type.

Sub a1 7

8. A semiconductor integrated circuit according to claim 6 or 7, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a potential in said well region, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

9. A semiconductor integrated circuit according to claim 6

or 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by the potential of said well region, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential of said well region.

10. A semiconductor integrated circuit according to claim 6 or 7, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of said well region, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

11. A semiconductor integrated circuit according to claim 6 or 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential in said well region.

12. A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source, a first pair of a high potential and a low potential; and

a second logic gate using, as an operation power source, a second pair of a high potential and a low potential having a potential difference larger than that of said first potential pair,

wherein a substrate potential of an MIS transistor in said first logic gate and that of an MIS transistor in said second logic gate are common to each other, and

at least said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential.

13. A semiconductor integrated circuit according to claim 12, wherein said first potential pair includes a first high potential and a first low potential, said second potential pair includes a second high potential higher than said first high potential and a second low potential lower than said first low potential, and said substrate potential is a high potential side substrate potential between said first and second high potentials and is a low potential side substrate potential between said first and second low potentials.

14. A semiconductor integrated circuit according to claim 12, wherein said first potential pair includes a first high potential and a first low potential, said second potential pair includes a second high potential higher than the first high

potential and a second low potential lower than said first low potential, said second high potential is used as a high potential side substrate potential, and said second low potential is used as a low potential side substrate potential.

15. A semiconductor integrated circuit according to claim 12, wherein said first potential pair includes a first high potential and a first low potential, said second potential pair includes a second high potential higher than the first high potential and said first low potential, a potential between said first and second high potentials is used as a high potential side substrate potential, and a potential higher than said first low potential is used as a low potential side substrate potential.

16. A semiconductor integrated circuit comprising:

a first logic gate connected to a first pair of a high potential line and a low potential line; and

a second logic gate connected to a second pair of a high potential line and a low potential line having a potential difference larger than that of said first potential line pair,

wherein a substrate potential line is commonly used for supplying a substrate potential to an MIS transistor of said first logic gate and for supplying a substrate potential to an MIS transistor of said second logic gate, and

at least said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential.

SUB D7

17. A semiconductor integrated circuit according to claim 16, wherein

said first potential line pair includes a first high potential line and a first low potential line,

said second potential line pair includes a second high potential line having a potential higher than that of said first high potential line and a second low potential line having a potential lower than said first low potential line, and

said substrate potential line is a high potential side substrate potential line having a potential between the potential of said first high potential line and the potential of said second high potential line, and is a low potential side substrate potential line having a potential between the potential of said first low potential line and the potential of said second low potential line.

18. A semiconductor integrated circuit according to claim 16, wherein said first potential line pair includes a first high potential line and a first low potential line,

said second potential line pair includes a second high potential line having a potential higher than that of the first

high potential line and a second low potential line having a potential lower than that of said first low potential line, and

said second high potential line is used as a high potential side substrate potential line, and said second low potential line is used as a low potential side substrate potential line.

19. A semiconductor integrated circuit according to claim 16, wherein said first potential line pair includes a first high potential line and a first low potential line,

said second potential line pair is a second high potential line having a potential higher than that of the first high potential line and is said first low potential line, and

said substrate potential line is a high potential side substrate potential line having a potential between the potential of said first high potential line and the potential of the second high potential line, and is a low potential side substrate potential line having a potential higher than the potential of said first low potential line.

20. A semiconductor integrated circuit having a circuit region in which a number of logic gates each having an MIS transistor are arranged on a semiconductor substrate,

wherein said circuit region has a well region shared by a substrate potential every conduction type of an MIS

transistor,

a first logic gate using, as an operation power source, a first pair of potentials having a relatively small potential difference and a second logic gate using, as an operation power source, a second pair of potentials having a relatively large potential difference are formed in said well region,

in said well region, a p-type well region in which an n-channel type MIS transistor is formed and an n-type well region in which a p-channel type MIS transistor is formed are adjacent to each other, and

metal lines for supplying said first pair of potentials, said second pair of potentials, and a substrate potential are arranged on said well region.

21. A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential, and

said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

22. A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a

substrate bias is applied in a reverse direction by said substrate potential, and

said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

23. A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential, and

said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

24. A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential.

25. A semiconductor integrated circuit comprising:

a first logic gate for generating a relatively small output signal amplitude by using a first potential pair as an operation power source; and

a second logic gate for generating a relatively large output signal amplitude by using a second potential pair as an operation power source,

wherein a substrate potential of an MIS transistor in said first logic gate and that of an MIS transistor in said second logic gate are common to each other.

26. A semiconductor integrated circuit according to claim 25, wherein said first logic gate includes a sequence circuit and a combinational circuit, said second logic gate includes a sequence circuit and a combinational circuit, a plurality of unit signal paths each leading from a sequence circuit to a sequence circuit at the next stage via one or a plurality of combinational circuits are provided, and said plurality of unit signal paths includes a unit signal path in which said first and second logic gates mixedly exist.

27. A semiconductor integrated circuit according to claim 26, wherein in a unit signal path in which said first and second logic gates exist mixedly, said second logic gate is disposed on the upstream side of said first logic gate.

28. A semiconductor integrated circuit according to claim 26, wherein in a unit signal path in which said first and second logic gates exist mixedly, a sequence circuit including said

second logic gate for receiving an output of a combinational circuit including said first logic gate has, at its input stage, a clock synchronous type level shifting circuit for shifting the level of an input signal amplitude to the level of an output signal amplitude of said second logic gate synchronously with a clock signal.

29. A semiconductor integrated circuit according to claim 26, wherein in a unit signal path in which said first and second logic gates exist mixedly, said second logic gate for receiving an output of said first logic gate is a level shifting circuit for shifting the level of an output signal amplitude of said first logic gate to the level of an output signal amplitude of said second logic gate, and a second logic gate circuit is connected to an output of said level shifting circuit in series.

30. A method of designing a semiconductor integrated circuit by using a first logic gate and a second logic gate in which substrate potentials of MIS transistors of the same conduction type are equal to each other, comprising:

a first step of determining whether a signal propagation delay time of a signal path in a logic circuit designed by using the first logic gate using, as an operation power source, a first pair of potentials having a relatively small potential difference achieves a target time or not; and

a second step of replacing one or a plurality of first logic gates included in a signal path having a signal propagation delay time which does not achieve the target time in said first step with a second logic gate using, as an operation power source, a second pair of potentials having a relatively large potential difference.

31. A method of designing a semiconductor integrated circuit according to claim 30, further comprising

a third step for determining whether a signal propagation delay time of the signal path in which replacement is performed in said second step achieves the target time or not and, if it does not achieve the target time, replacing another first logic gate included in the signal path with a second logic gate.

32. A method of designing a semiconductor integrated circuit according to claim 31, wherein in said second and third steps, the replacement with the second logic gate is performed from the upstream side of the signal path.

33. A method of designing a semiconductor integrated circuit according to claim 31, wherein in said second and third steps, when the second logic gate as a sequence circuit is disposed at the next stage of a first logic gate, said second logic gate has, at its input stage, a clock synchronous type level shifting

function for shifting the level of an input signal amplitude to the level of an output signal amplitude of the second logic gate synchronously with the clock signal.

34. A method of designing a semiconductor integrated circuit according to claim 31, wherein in said second and third steps, when the second logic gate is disposed at the next stage of the first logic gate, a level shifting circuit for shifting the level of an output signal amplitude to the level of an output signal amplitude of the second logic gate is inserted in front of said second logic gate.

35. A program recording medium on which a program for supporting designing of a semiconductor integrated circuit using a first logic gate and a second logic gate in which a substrate potential of MIS transistors of the same conduction type are equal to each other is recorded so as to be read by a computer, the program executing:

a first step of determining whether a signal propagation delay time of a signal path in a logic circuit designed by using the first logic gate using, as an operation power source, a first pair of potentials having a relatively small potential difference achieves a target time or not; and

a second step of replacing one or a plurality of first logic gates included in a signal path having a signal

propagation delay time which does not achieve the target time in said first step with a second logic gate using, as an operation power source, a second pair of potentials having a relatively large potential difference.

36. A program recording medium according to claim 35, wherein said program can further execute a third step for determining whether a signal propagation delay time of the signal path in which replacement is performed in said second step achieves the target time or not and, if it does not achieve the target time, replacing another first logic gate included in the signal path with a second logic gate.

37. A design data recording medium on which design data for designing an integrated circuit to be formed on a semiconductor chip by using a computer is recorded so as to be read by said computer, the design data comprising:

first mask pattern data for determining a figure pattern for forming a first logic gate to which an operation power source is supplied from a first pair of potential lines having a relatively small potential difference and a substrate potential is supplied from a substrate potential line on said semiconductor chip; and

second mask pattern data for determining a figure pattern for forming on said semiconductor chip a second logic gate to

which an operation power source is supplied from a second pair of potential lines having a relatively large potential difference and a substrate potential is supplied from a substrate potential line.

38. A design data recording medium on which design data for designing an integrated circuit to be formed on a semiconductor chip is recorded so as to be read by said computer, the design data comprises:

first function description data for determining a function of a first logic gate to which an operation power source is supplied from a first pair of potential lines having a relatively small potential difference and a substrate potential is supplied from a substrate potential line; and

second function description data for determining a function of a second logic gate to which an operation power source is supplied from a second pair of potential lines having a relatively large potential difference and a substrate potential is supplied from a substrate potential line connected to said substrate potential line.

add a2

add